APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: FOCUSED ION BEAM VISUAL ENDPOINTING

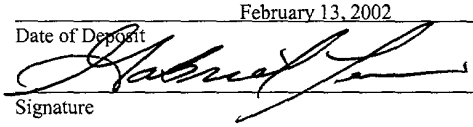
APPLICANT: SAILESH C. SUTHAR, PAUL J. HACK, SYED NABEEL SARWAR AND MARY J. MARTINEZ

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EL870691517US

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail Post Office to Addressee with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

February 13, 2002
Date of Deposit



Signature

Gabriel Lewis
Typed or Printed Name of Person Signing Certificate

FOCUSED ION BEAM VISUAL ENDPOINTING

TECHNICAL FIELD

The application relates, generally, to integrated circuit processing and, more particularly, to endpoint detection for ion beam etching.

BACKGROUND

During product development of integrated circuits, prototype circuits can be physically edited to debug an integrated circuit design. Circuit editing involves an alteration of interconnect routing by, e.g., drilling vias through a backside of a chip to interconnections in the chip and depositing metal in the vias to alter the connections between device active areas. Devices on a chip can thereby be connected in alternative ways, facilitating post-processing troubleshooting.

Prior to the formation of this type of via, the backside of a silicon chip is thinned by, e.g., focused ion beam etching, also known as ion milling. Typically, a timed etch is performed based on the expected etch rate and the expected silicon thickness. A timed etch can be problematic, especially in the case of variable etch rates

and silicon thicknesses. The thickness of silicon remaining after a timed etch typically falls within a wide range such as 4 - 5 microns (μm) $\pm$ 2 μm, leading to unreliability in subsequent processing, such as via formation. Further, thinning the chip too much can damage the device which one wishes to contact. For example, etching into a diffused region can adversely affect device performance.

An alternative to timed etching includes photo current endpoint/real time optical beam induced current (PCEP/RT-OBIC) technique. This technique has the drawback of requiring the installation of additional hardware. A further limitation of the PCEP/RT-OBIC technique is that it does not provide an endpoint curve if the area being milled has >30% decoupling capacitors, i.e. capacitors for noise filtering, or if the mill box size, i.e. the area scanned by an ion beam during etching, is less than 100 μm x 100 μm.

DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view of a silicon substrate being milled from its backside, according to an embodiment;

Fig. 2 is a top view of the backside of the silicon substrate of Fig. 1; and

Fig. 3 is a top view of a backside of a silicon substrate, as displayed in a monitor.

DESCRIPTION

An endpointing method enables one to consistently stop etching a backside of a silicon chip within a distance of approximately 2 μm from a bottom portion of a diffused region. A focused ion beam induces a charge in a p-well proximate an n-well when the beam etching the backside of the chip comes within 2 μm of the diffused regions. The etching can be stopped at that point. Subsequently, vias can be formed to contact interconnects in the chip.

Referring to Fig. 1, a semiconductor chip 10 (shown upside down with a backside 22 facing upward) has an epitaxial layer 12 formed over a silicon substrate 14. Semiconductor chip 10 is packaged such that backside 22 of silicon substrate 14 is exposed. Suitable packaging (not shown) is a control collapsed chip carrier (C4). Epitaxial layer 12 has, e.g., p-type doping and a thickness T_1 of 2.75 μm. In some embodiments, T_1 is selected from a range of 2 μm - 3 μm. An n-well 16 and a p-well 18 (see also Fig. 2) are formed in epitaxial layer 12 by, for example, the

implantation of n-type ions and p-type ions, respectively. Bottom portions of n-well 16 and p-well 18 form an n-well junction 19 and a p-well junction 19' in epitaxial layer 12, respectively. Typically, junctions 19, 19' have a depth D_1 equal to approximately 80 - 90% of the thickness T_1 of epitaxial layer 12. N-well 16 and p-well 18 have, for example, junction 19, 19' depths D_1 of approximately 2.4 μm.

A shallow trench isolation (STI) region 20 is formed between n-well 16 and p-well 18. STI region 20 includes a dielectric such as silicon dioxide that provides electrical isolation between portions of n-well 16 and p-well 18 proximate to STI region 20. A thickness T_2 of STI region 20 is approximately one-third of the thickness T_1 of epitaxial layer 16. Thickness T_2 of STI region 20 is, for example, 0.9 μm.

Backside 22 of silicon substrate 14 has been globally thinned from an initial thickness of about 775 μm to about 100 μm. This global thinning can be done in a polishing/grinding system. Subsequently, a localized area 24 over n-well region 16 and p-well region 18 was thinned to leave a thickness of about 10 μm - 15 μm of silicon substrate 14/epitaxial layer 12 above junctions 19, 19'. Localized thinning can be done in a laser-chemical etching system.

Subsequent to localized backside thinning, semiconductor chip 10 is loaded into a focused ion beam (FIB) system (not shown) for backside etching. Focused ion beam system is, for example, a Vectra™ 986 system manufactured by FEI Company of Hillsboro, Oregon. Upon being loaded into the FIB system, a front side 24 of semiconductor chip 10 is coupled to FIB system's connection 26 to ground potential.

A gallium ion beam 28 further etches backside 22 of silicon substrate 14 over n-well 16 and p-well 18, i.e. gallium ion beam 28 etches back localized thinned area 24. Gallium ion beam 28 has a relatively high current ranging from, e.g., 8 nanoamperes to 19 nanoamperes. Spot size 30 has an area A_1. In the case where gallium ion beam 28 current is 19 nanoamperes, A_1 is approximately 1 - 2 square microns (μm^2). A xenon difluoride (XeF_2) gas flux is used in conjunction with gallium ion beam 28. XeF_2 is introduced at a flow rate sufficient to cause a pressure loss in an etch chamber (not shown) equivalent to approximately 1 - 2 Torr. XeF_2 accelerates etching of backside 22 by providing fluorine ions to react with silicon substrate 14. If gallium ion beam 28 current is 19 nanoamperes, an etch rate of silicon substrate 14 is 1.0x10E5 to 1.8x10E5 cubic micrometers/minute (μm^3/min).

Localized thinned area 24 is etched back by gallium ion beam 28 until silicon substrate backside 22 is within a distance D_2 from junctions 19, 19'. D_2 is, for example, 2 μm. In some embodiments, D_2 is approximately 1.5 to 3 μm.

The moment that distance D_2 from junctions 19, 19' is reached is determined as follows. During focused ion beam etching, gallium ion beam 28 induces a positive charge 32 in silicon substrate 14. This positive charge 32 is induced by positively charged ions comprising gallium ion beam 28. N-well 16 in epitaxial layer 12 has a relatively high resistivity of approximately 1000 ohms-cm and is capacitively coupled to a source voltage (V_{ss}) (not shown). The resistivity and capacitive coupling of n-well 16 reduces the possibility of an ion discharge of a positive charge 34 built-up in epitaxial layer 12 and positive charge 32 built up in silicon substrate 14 over n-well 16, thereby creating a brighter region in an image 40 on a monitor (see discussion below with reference to Fig. 2). On the other hand, p-well 18 has a lower resistivity than n-well 16, e.g., approximately 500 ohm-cm. This lower resistivity allows positive charges 32 induced over p-well 18 to dissipate relatively quickly, thereby creating a darker region in image 40 on the monitor (see discussion below with reference to Fig. 2).

Referring also to Fig. 2, during the etching of silicon substrate 14, image 40 of backside 22 is transmitted to the monitor. Image 40 on the monitor corresponds to a portion 42 of backside 22 upon which gallium ion beam 28 impinges. Image 40 is formed by the detection of secondary electron emission from silicon substrate 14 induced by gallium ion beam 28. The positive charge 34 build-up over n-well 16 reduces secondary electron emission over n-well 16. The discharge of positive charge 32 over p-well 18, however, increases secondary electron emission over p-well 18.

As gallium ion beam 28 induces etching of silicon substrate 14 and gallium ion beam 28 approaches within distance D_2 of approximately 2 μm from junctions 19, 19' by thinning silicon substrate 14, the difference between secondary electron emission over n-well 16 and p-well 18 becomes visible. The low secondary electron emission over n-well 16 appears as a dark area in image 40, while the higher secondary electron emission over p-well 18 appears as a bright area, in contrast to n-well 16. To show the required contrast between n-well 16 and p-well 18, the monitor is calibrated with 256 gray levels.

A person or computer operating the focused ion beam system, upon determining the presence of contrast in

brightness between n-well 16 and p-well 18, stops the focused ion beam etching by turning off gallium ion beam 28. This contrast becomes visible only when a distance D_2 is approximately 2 μm or less, i.e. when $\leq$ 2 μm of silicon is left above junctions 19, 19' of n-well 16 and p-well 18, respectively. By stopping the focused ion beam etching at the point when the contrast first appears, one can consistently thin backside 22 of semiconductor chip 10 to a thickness D_2 of approximately 2 μm over n-well 16 and p-well 18.

After the completion of the thinning of silicon substrate 14 by focused ion beam etching, a circuit on semiconductor chip 10 is edited, i.e. electronic routing is physically altered. A via (not shown) is formed through a remaining portion of silicon substrate 14 and epitaxial layer 12 in an inactive area to contact an interconnect (not shown). Vias are filled with metal plugs (not shown), and interconnections (not shown) are formed between metal plugs to modify electronic routing between devices on semiconductor chip 10. The same focused ion beam system which is used for focused ion beam etching can be used to form these vias, metal plugs, and interconnections.

Referring also to Fig. 3, an image 50 appears on a monitor 52 when gallium ion beam 28 impinges on

semiconductor chip 10 (see Fig. 1). Image 50 includes an entire area of semiconductor chip 10 backside 22 which is contacted by gallium ion beam 28. As noted above with reference to Fig. 1, gallium ion beam 28 has a relatively high beam current of 8 nanoamperes - 19 nanoamperes with a correspondingly relatively large spot size 30 with area A_1 of, for example, 1 - 2 μm^2. Further, gallium ion beam 28 is scanned back and forth across a portion of backside 22, covering an area having a mill box size of, for example, 250 μm x 250 μm. Gallium ion beam 28 impinges, therefore, simultaneously on a number of n-wells 16, 16', and p-wells 18, 18'. For the reasons described above with reference to Figs. 1 and 2, n-wells 16, 16' appear on monitor 52 as dark areas and p-wells 18, 18' appear on monitor 52 as bright areas, after the silicon above the junctions 19, 19' of n-wells 16, 16' and p-wells 18, 18' is thinned to approximately 2 μm. Once this point is reached, focused ion beam etching can be stopped and connections between transistors (not shown) within n-wells 16, 16' and p-wells 18, 18' can be modified by well-known circuit editing procedures, as mentioned above with reference to Fig. 2.

The method is not limited to the specific embodiments described above. For example, other focused ion beam systems can be used, manufactured by companies such as

Hitachi, Schlumberger, etc. The described method can be used as an endpoint detection method for etching any substrate that has two regions with two types of doping, including an n- or a p-well combined with an intrinsic semiconductor such as undoped silicon. The semiconductor chip can be etched with a material other than gallium ions, such as another type of ion beam or an electron beam. In the case of etching with a negatively charged beam, the n-wells will appear brighter than the p-wells.

Embodiments of the described endpoint detection method can find applicability in various computing and processing environment. An embodiment of the endpoint detection method may be implemented in computer programs executing on programmable computers or other machines that each include a processor, a storage medium readable by the processor (including volatile and non-volatile memory and/or storage components), at least one input device, and one or more output devices. Program code may be applied to data entered using an input device (e.g., a mouse or keyboard) to perform embodiments of the endpoint detection method and to generate output information. Each such program may be implemented in a high level procedural or object-oriented programming language to communicate with a computer system. However, the programs can be implemented in assembly or

machine language. The language may be a compiled or an interpreted language.

Each computer program may be stored on a storage medium/article (e.g., CD-ROM, hard disk, or magnetic diskette) that is readable by a general or special purpose programmable computer for configuring and operating the computer when the storage medium or device is read by the computer to perform embodiments of the endpoint detection method. An embodiment of the endpoint detection method may also be implemented as a machine-readable storage medium, configured with a computer program, where, upon execution, instructions in the computer program cause a machine to operate in accordance with an embodiment of the endpoint detection method.

A computer can be programmed to etch semiconductor chip 10, monitor the backside of semiconductor chip 10 during etching, determine when a first portion of the backside over one of first and second wells in the frontside of chip 10 differs from a second portion of the backside over the other of the first and second wells.

The semiconductor chip 10 may be formed on a substrate formed from a material other than silicon, such as gallium arsenide or another material. Instead of a completed semiconductor chip 10, the endpoint detection method can be

used with any semiconductor substrate having a first region with a first type of doping and a second region with a second type of doping. The first or the second region can be an undoped intrinsic semiconductor region.

Other embodiments not described herein are also within the scope of the following claims.

What is claimed is: